IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). In addition to the amendment of claims 1 and 2 (shown herein as entered) in the Amendment filed November 5, 2004, please CANCEL claims 7-9 without prejudice or disclalimer, in accordance with the following:

1. (previously presented) A semiconductor package, provided with a multilayer interconnect structure, for mounting a semiconductor chip on its top surface, wherein:

a topmost stacked structure of the multilayer interconnect structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of a high dielectric constant inorganic filler and an insulating resin and including chip connection pads for directly connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip,

wherein the dielectric layer is selectively provided only on an electrode of the capacitor structure.

2. (previously presented) A semiconductor package, comprised of an insulating substrate on top and bottom surfaces of which multilayer interconnect structures are provided, for mounting a semiconductor chip on the top surface of a top surface multilayer interconnect structure, wherein:

the top surface multilayer structure includes a capacitor structure, said capacitor structure having a dielectric layer comprised of a mixed electrodeposited layer of a high dielectric constant inorganic filler and an insulating resin, and a topmost layer of said top surface multilayer interconnect structure includes chip connection pads for connecting top electrodes and bottom electrodes with electrodes of said semiconductor chip inside a region superposed with said capacitor structure in a plan view,

wherein the dielectric layer is selectively provided only on an electrode of the capacitor structure.

3. (previously presented) A semiconductor package as set forth in claim 2, wherein

said top surface multilayer interconnect structure includes a plurality of stacked capacitor structures.

4. (previously presented) A semiconductor package as set forth in claim 1, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

5. (previously presented) A semiconductor package as set forth in claim 1, wherein said insulating resin is a polyimide resin.

6. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 1 and a semiconductor chip directly connected at its electrodes to the chip connection pads.

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (previously presented) A semiconductor package as set forth in claim 2, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

11. (previously presented) A semiconductor package as set forth in claim 3, wherein said inorganic filler is a powder of ceramic having a perovskite structure.

12. (previously presented) A semiconductor package as set forth in claim 2, wherein said insulating resin is a polyimide resin.

13. (previously presented) A semiconductor package as set forth in claim 3, wherein said insulating resin is a polyimide resin.

14. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 2 and a semiconductor chip directly connected at its electrodes to

the chip connection pads.

15. (previously presented) A semiconductor device comprised of a semiconductor package as set forth in claim 3 and a semiconductor chip directly connected at its electrodes to the chip connection pads.